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Seed Enhancement: A Bridging Technology

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With ultra-large-scale integration progress, efficient copper metallization of the narrow features becomes challenging. Among the elementary steps involved in the metallization sequence, the most critical will probably be the deposition of a copper seed layer necessary to initiate the bulk copper electrochemical deposition (ECD). For future generations, physical vapor deposition (PVD) techniques that are currently employed will reasonably reach a limit, as they are not able to perfectly cover the sidewalls of the features. The resulting discontinuous seed layers can cause defects such as voids in the copper lines and contact holes. To overcome this, "seed enhancement" or "seed repair" techniques have been proposed, which are able to bridge the local discontinuities of the copper PVD layer. In this article, this concept is illustrated through the example of an electrodeposition process called ECD seed™. The benefits of this approach are demonstrated, and the remaining challenges are discussed.

Introduction

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Introduction

The successful introduction in the late 1990s of copper as the conductive medium in chip interconnects was the result of two major achievements: the finding of suitable barrier materials deposited by PVD and the adoption of electrochemical deposition to efficiently fill the inlaid submicron features. Since then, much attention was paid to the sophistication of the ECD solutions, in order to extend the filling performances of these processes.[1,2] More recently, barrier layers have gained renewed interest, with the apparition of atomic layer deposited (ALD) barriers.[3] This new deposition technique provides highly conformal, ultra-thin layers that can fulfill the requirements of the next technological generations. Surprisingly, much less emphasis was put on the copper seed layer deposition. This thin metallic liner is necessary to ensure uniform (at the wafer scale) and continuous (inside the feature) transport of the current during the initial stages of ECD. Just as for the barrier layer, copper seeding by PVD techniques will become challenging in features at sub- 0.1 µm dimensions. For this reason, an evolution of the copper seeding processes will be necessary.

This article focuses on the "seed enhancement" or "seed repair" approach, which was proposed to extend the use of PVD seed layers that may become discontinuous in the narrow structures. More precisely, we will illustrate the concept and possibilities of this approach through a specific example, the ECD seed™ process proposed by Semitool.[4]

The Concept of Seed Enhancement

As feature size is shrinking below 0.1 µm, seed layer deposition for efficient electroplating becomes a critical step in the damascene approach. Ideally, a seed layer should be thin to leave sufficient space inside the features for copper filling, and conformal to ensure efficient conduction and copper deposition at the bottom of the geometries. With PVD techniques, which usually form an overhang at

the mouth of the features, seed layer thickness must not exceed a few tens of nanometers to leave enough space for copper filling. With imperfect step coverage of the PVD techniques, such thin seed layers will probably not be continuous on the sidewalls. These discontinuities lead to the formation of characteristic “bottom voids” during ECD filling.

Alternative conformal deposition techniques are studied to overcome this technological limit. Copper CVD was demonstrated to yield efficient seeding, with conformal and ultra-thin films.[5] However, a limitation of this technique is still the weak adhesion between copper and the underlying barrier. Copper ALD has not emerged yet as a solution, mainly due to the challenging conversion of the ALD-grown copper oxide into metallic copper.[6]

By contrast with the process revolution implied by these two techniques, seed enhancement appears to be a more accessible and immediate process evolution. The central idea of this approach is to “repair” the PVD seed layer by bridging its discontinuities inside the features. For this purpose, wet chemical processes have been proposed that can be easily implemented in current plating tools.[7] In this way, the addition of the seed enhancement step in the metallization sequence can be quite straightforward.

The ECD Seed™ process

In this article, we present results obtained using an electrolytic process called ECD seed™.[4] This process, developed by Semitool, is very similar to standard electroplating; the same deposition chambers and comparable current protocols are used. The main difference is in the composition of the bath. By contrast with conventional acidic ECD solutions, this chemistry is designed to grow copper not only on the seed layer, but also locally on the barrier material, and to limit corrosion of the PVD copper in the first stages of the deposition.

The latter property of this solution was assessed by quartz microbalance measurements. The etch rate of copper under open circuit potential was found to be limited to a few angstroms per minute. Under cathodic polarization, copper is deposited with a faradic efficiency of 95 percent, which contrasts with standard electroplating solutions, for which this efficiency is close to 100 percent. This indicates that side reactions occur during deposition of the ECD seed layer, possibly hydrogen evolution.

The physical and chemical properties of the deposits were found to be dependent not only on the process conditions, but also on the underlying barrier and seed. On one hand, properties such as surface roughness or density of the film are conditioned by the current density applied during deposition. On the other hand, adhesion and texture are mainly dependent on the barrier and seed stack. More precisely, films grown on PVD TaN/Ta substrates are found to be highly (111) textured.

Step Coverage and Feature Filling

The ability to efficiently cover the sidewalls of narrow features is a key property for a seed enhancement process. In the case of the ECD seed process, the electrolytic deposition has to be very conformal (no overdeposition in the upper part of the features), but also be able to bridge the discontinuities in the copper seed - that is to say to deposit directly on the barrier (at least at short distance). Both aspects are challenging with a current-driven deposition such as ECD seed. The sharp edges of the features tend to attract current density during electrodeposition, resulting in the accumulation of matter at the top of the features. The transition between a conductive copper and a more resistive barrier surface is likely to induce a diminution of the local current density (and local deposition rate), due to local ohmic drop effect in areas where the barrier is exposed.

Aggressive conditions to evaluate the step coverage capabilities of the ECD seed process are thus to use dense structures of narrow features with an extremely thin copper seed layer. Typical results obtained in 0.12/0.12 µm width/space trench arrays covered with 15 nm non-collimated PVD copper seed are presented in Figure 1.

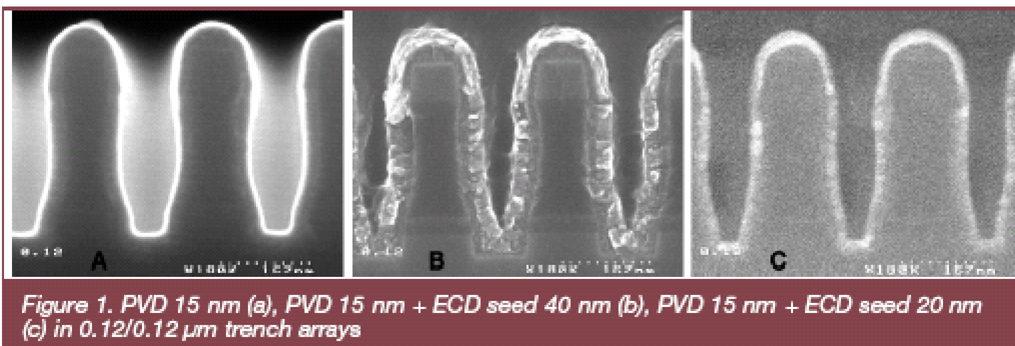


Figure 1. PVD 15 nm (a), PVD 15 nm + ECD seed 40 nm (b), PVD 15 nm + ECD seed 20 nm (c) in 0.12/0.12 µm trench arrays

With such a thin seed (the typical thickness for a seed is 100 nm) deposited by non-collimated PVD (more advanced techniques are usually used to allow improved step coverage), it is expected that almost no copper is deposited on the sidewalls of the trenches. Even

under such conditions, the ECD seed process is efficient. Figure 1b shows that conformal layers are obtained that are perfectly continuous inside the features. The fact that the deposition is active on the poorly seeded areas as soon as current is turned on is more clearly evidenced in Figure 1c: a 20 nm thick film is already continuous on the sidewalls. This is confirmed by experiments conducted in 80 nm-wide trenches (see Figure 2).

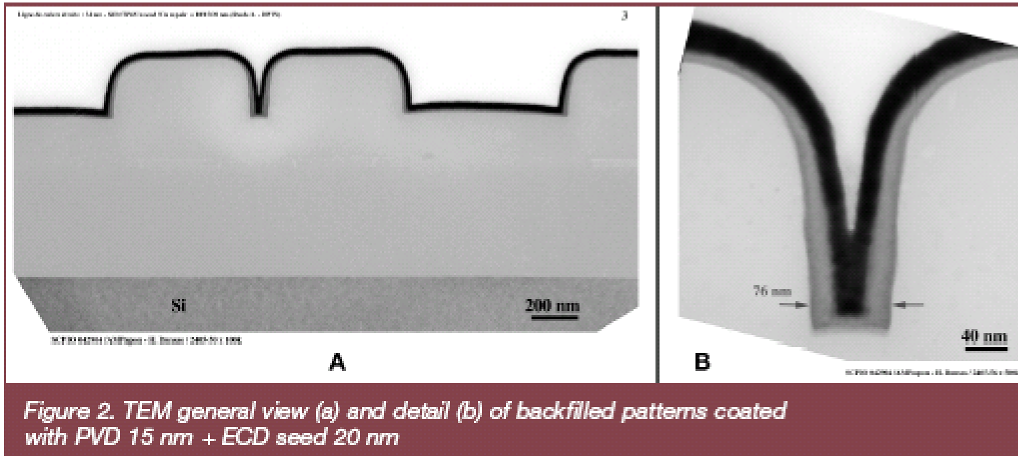


Figure 2. TEM general view (a) and detail (b) of backfilled patterns coated with PVD 15 nm + ECD seed 20 nm

More evidence of the efficiency of the seed enhancement approach is given in Figure 3.

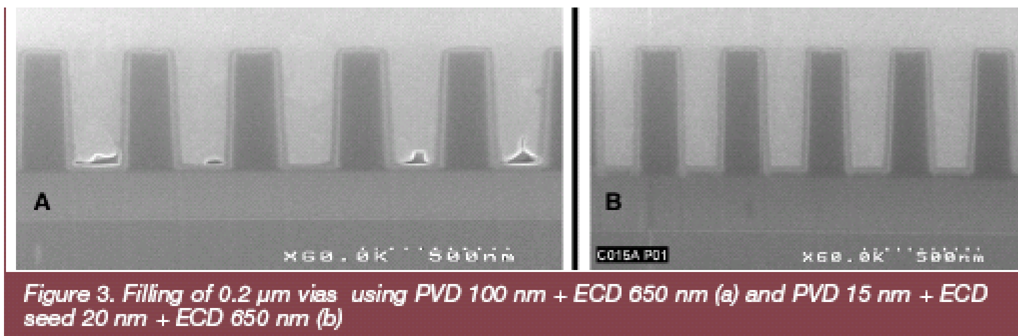


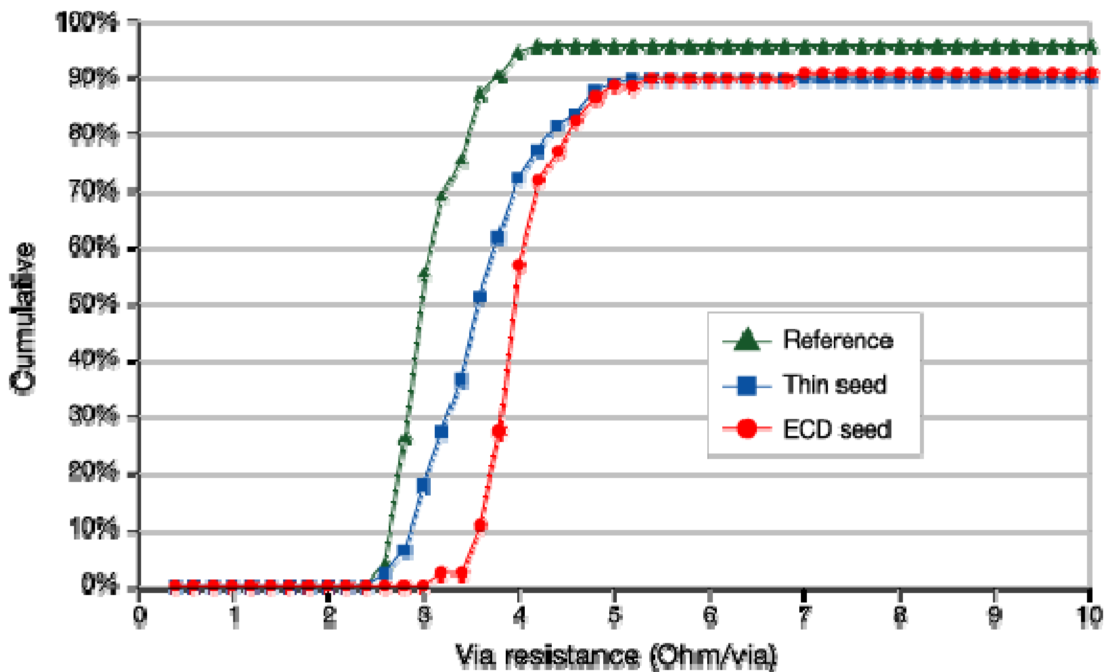
Figure 3. Filling of 0.2 µm vias using PVD 100 nm + ECD 650 nm (a) and PVD 15 nm + ECD seed 20 nm + ECD 650 nm (b)

In this experiment, 0.2 µm vias were examined, with two different copper seed layers: a 100 nm-thick non-collimated PVD film, and the 15 nm PVD + 20 nm ECD seed described above. After copper filling, systematic bottom voids are present in the PVD-seeded vias, as expected. Conversely, excellent filling of the vias processed through ECD seed is obtained. This clearly confirms that the ECD seed process is able to plate copper on poorly seeded areas where traditional ECD solutions are not.

Integration of Seed Enhancement in the Metallization Sequence

To carry out the filling experiments described above, no modification of the electroplating process was necessary. In other words, the filling improvement can be obtained through straightforward incorporation of the seed enhancement step in the metallization sequence.

However, the successful implementation of such a seed repair process remains challenging. To illustrate this, let us consider via resistance results plotted in Figure 4.



In these experiments, three different copper seed layers are considered: a 120 nm-thick copper seed deposited by self-ionized plasma (SiP) PVD (reference); a thinner 80 mn SiP seed layer; and an ultra-thin 20 nm SiP seed layer followed by 20 nm ECD seed. As expected, the thinning of the copper seed down to 80 nm causes via resistance increase and yield loss as compared to the reference. The wafers processed with the ECD seed exhibit a similar yield loss, with a still higher via resistance. Considering that the initial seed was only 20 nm thick, this result is quite encouraging. However, under optimal seed enhancement conditions, no negative impact on via resistance and yield is expected.

This degradation of these electrical performances may have several causes. The presence of contaminants in the ECD seed layer may contribute to the resistance increase. SIMS analyses have shown the presence of organic contaminants, probably due to incorporation of organic components of the deposition bath. More important is probably the impact of oxidation of the seed layer and exposed barrier material during queue time between copper seed deposition and ECD seed plating. If copper oxide is possibly converted into metallic copper during the cathodic deposition process, it is probable that oxidized barrier remains after seed enhancement, especially at the bottom of the vias. This resistive oxide is likely to contribute to the degradation of the conduction properties of the vias.

Thus, the efficient integration of a seed enhancement process into the metallization scheme still needs to be demonstrated. To preserve electrical performances and maintain a low level of defects, some optimization has to be achieved. In particular, the limitation of oxidation of the barrier and copper surfaces prior to seed enhancement is probably a key challenge.

Conclusion

With the reduction of feature size in the coming technological nodes, limited step coverage of the PVD techniques used to deposit barrier, and seed layer is anticipated to yield discontinuous films. If ALD is actively developed for barrier deposition, no solution has clearly been defined yet concerning copper seeding. In this article, we discuss the concept of seed enhancement to extend the use of PVD seeding. Through the example of ECD seedTM, the benefits of this approach are demonstrated. The seed repair process clearly improves copper seeding of the sidewalls and bottom of the narrow features. However, several challenges remain for efficient introduction of this process into the metallization sequence. In particular, the oxidation of the exposed barrier and ultra-thin portions of the seed during queue time prior to seed repair are pointed out as potential issues.

Seed enhancement is a bridging technology, in the sense that the use of PVD techniques may be extended until a deeper process revolution is required. It is also a possible pathway to achieve this process revolution: a conformal deposition technique that is able to locally cover exposed barrier material is a good starting point in the quest of a copper seeding process by a wet chemical process.

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