Presented at IMAPS-Device Packaging, March 13-16, 2005, Hilton Scottsdale Resort & Villas, Scottsdale, AZ, USA

Factors Limiting the Electrodeposition Rate of Various Bumps for Flip-Chip Interconnects

Bioh Kim, Bob Batz, and Tom Ritzdorf
Semitool, Inc.
655 West Reserve Drive
Kalispell, MT, 59901
Phone : 406-752-2107, Fax : 406-751-6371, E-mail : bkim@semitool.com

Abstract

We developed various high-rate bump processes and examined factors limiting the maximum deposition rate in each process (Cu, Ni, eutectic SnPb, and eutectic SnAg). In order to achieve higher deposition rate while maintaining deposit qualities, numerous factors should be considered along with the limiting current density (LCD) of the process. The maximum rate of eutectic SnPb solder deposition was significantly reduced by the probability of abnormal growths. This problem was dependent upon bath composition, which limited bath makeup and thus reduced LCD and resultant maximum rate. In the case of Cu stud deposition, the deposit qualities at high deposition rates were greatly affected by organic composition. Most organic additives showed poor functionality at high deposition rates. With an optimized bath, the current crowding at high current density areas was the major limiting factor, causing rough deposits and poor within-die thickness uniformity. Due to poor throwing power of the Ni bath, within-die thickness uniformity was barely acceptable at 2-3μm/min, even though no big change in growth shape and morphology was observed up to 7μm/min. Inert anodes were used for eutectic SnAg solder deposition due to the displacement reaction. Gas generation from the anodes significantly limited the operating range of current density. However, in all cases, we achieved acceptable rates with a tested pattern, ranging from 2 to 6μm/min depending upon process type.

Key words : through-mask deposition, maximum deposition rate, eutectic SnPb solder, eutectic SnAg solder, Cu stud, and Ni stud

Introduction

Mounting is a critical step in manufacturing electronic devices. As the devices are miniaturized and the circuitry becomes complicated, flip-chip (FC) technology is preferred over the conventional wire bonding or tape automated bonding. The advantages of FC technology include high-density bonding, gang bonding, improved electrical performance, self-alignment, reliability and manufacturability [1]. Solder bumps in FC interconnects serve as the electrical connector, mechanical supporter, and heat dissipator. Typical process schemes for producing solder bumps on wafers include the screen printing of solder pastes, solder ball (preform) placement, the evaporation of solder alloy (for instance, high-Pb PbSn) through a perforated stencil, and the through-mask deposition of desired metals and alloys. The most practical, cost-effective method for producing fine-geometry bumps is through-mask deposition [2-14].

The theoretical deposition rate is a function of charge-transfer kinetics at the metal-electrode interface and mass transfer through the diffusion layer [15]. The higher the deposition rate, the higher the throughput. In order to achieve high deposition rate for practical through-mask deposition while maintaining deposit qualities, a variety of factors should be considered together with the LCD of the process. Those factors include (*i*) mask properties such as open area, mask thickness, and pattern configuration, (*ii*) within-wafer (WIW) and within-die (WID) uniformity of thickness and composition, (*iii*) surface roughness, morphology, and growth shape along the feature location, (*iv*) abnormal growths such as nodules, columns, or dendrites, and (*v*) gas generation from the anodes in the case of using inert anodes, etc.

This paper reviews the previous work that studied different high-rate bumping processes (Cu stud, Ni stud, eutectic SnPb solder, and eutectic SnAg solder) using a fountain-type reactor. The focus of

this work was to describe the important rate-limiting factors for various processes.

Template Properties vs. LCD and Growth Shape

The LCD is of great importance in electrodeposition. Not only do the type and quality of deposits depend upon the ratio of applied current density to LCD (or %LCD), but also the range of operating current density is defined by the LCD. The higher the LCD, the wider the current density operating range. The LCD was enhanced by increasing metal concentration and by decreasing acid concentration [13,16]. With increasing agitation and bath temperature, the LCD was also increased.

In the case of through-mask deposition, the effects of template properties on the LCD (and resultant growth shape) should be considered [17]. With increasing open area and template thickness, the LCD decreases and hence the achievable deposition rate decreases due to the onset of columnar and dendritic growths. Pattern configuration also has a significant effect on the current distribution within a die. This can limit the maximum deposition rate due to the variation of deposit properties (for instance, thickness, morphology, and shape) along feature locations. As shown in Figure 1, the current distribution within a die became less uniform with increasing current density.

With increasing %LCD, the growth shape became more influenced by pattern parameters (and flow conditions). The effect of feature diameter and deposit thickness at high %LCD (approximately, 60-70%) on the growth shape of copper studs is illustrated in Figure 2. The variation of peak thickness location was observed with increasing feature diameter [18-20]. The growth shape became more apparent with thicker deposits and thus became more skewed along flow direction.

Mask surface treatment conditions, including plasma-ashing with reactive gases, aging in the air after plasma-ashing, and pre-wetting with surfactant-containing solutions influenced the surface energies of the mask-electrolyte interface as well as the mask itself. This phenomenon also affected the growth shape of deposits [17]. When the resist has insufficient surface energy or is aged for a long time after surface treatment, the shape ratio of deposits, which is defined as the ratio of the thickness at the cavity edge to the thickness at the cavity center, tends to decrease [11,17]. Figure 3 shows the impact of wafer aging after plasma-ashing on the feature-scale growths. With aging, the surface profile became more domed and skewed along the flow direction.

Experimental Methods

Table 1 summarizes the baths used for this work. We used a potentiostat (EG&G model 263A with EG&G 270 software) was used for linear-sweep voltammetry with a rotating disc electrode (RDE) to examine bath composition impact on the LCD. 200mm-patterned wafers had the structure of Si(substrate)/SiO_2/ Ti/PVD-Cu/mask, where Clariant AZ 4620 was used as the photoresist. The parameters of the single pattern (named as pattern-A) are summarized in Table 2.

We used the following hardware: (*i*) Semitool's fountain-type reactor with multiple anodes to examine the factors limiting the maximum deposition rate, (*ii*) a focused ion beam (FIB, FEI dual beam 820) to observe surface morphology and growth shape, (*iii*) an energy-dispersive spectrometer (EDS, Noran Voyager) or X-ray fluorescence spectroscopy (XRF) to examine alloy composition, and (*iv*) a surface metrology tool (Veeco Dektak 300-Si) to measure deposit thickness. We fixed mass-transfer-related factors after examining the effects of rotation speed, flow rate, and bath temperature on the LCD, growth shape, resist stability, and hardware stability.

Table 1. Baths used for this work.

Process	Bath	Acid Type
Cu	Rohm and Haas Intervia 8540	Sulfuric-based
Ni	Rohm and Haas Nikal BP	Sulfamate-based
Eutectic SnPb	Rohm and Haas Solderon BP	MSA-based
Eutectic SnAg	MMC UTB TS-140	MSA-based

Table 2. Pattern parameters of pattern-A.

Parameters	Values
Feature Shape	Via
Number of Vias in a die	1,521 (39×39)
Open Area	16.5%
Mask Thickness	55μm
Via Diameter	130μm
Via Pitch	250μm
Distance between Dice	~1,000μm

Experimental Results and Discussion

For each process, we examined a variety of factors to define the primary rate-limiting factors for various processes. These factors include (*i*) the LCD of process, (*ii*) WIW and WID uniformity of thickness and composition, (*iii*) surface roughness, morphology, and growth shape along the feature location, (*iv*) abnormal growths such as nodules, columns, or dendrites, and (*v*) gas generation from the anodes in the case of using inert anodes.

I. Eutectic SnPb Solder Deposition

Full details on the development of high-rate eutectic SnPb solder process are summarized in References [11,13]. The LCD of eutectic SnPb baths was significantly raised by increasing metal concentration and decreasing acid concentration, as shown in Figure 4. A change of morphology and growth shape with increasing deposition rate was small up to 10μm/min [13]. At the wafer centers, the surface became slightly rougher at 9μm/min and the growth shape started to change from 10μm/min. This is due to the wafer rotation and pattern effects on the LCD. The thickness and composition uniformity, measured up to 8μm/min, was acceptable.

However, the use of this bath was significantly limited by the probability of abnormal growths. Figure 5 shows the typical abnormal growths (with one or more nodules on solder bumps) observed frequently from the eutectic SnPb solder bumps [11,13]. The cross-section of an abnormally grown area showed no significant difference in grain morphology compared with a normally grown area. The mechanism of this type of abnormal growth is not fully understood, but some process conditions such as bath composition, deposition rate, waveform, and bath aging are proven experimentally to influence the probability of this type of abnormal growth. As shown in Figure 6(a), the probability of abnormal growths was significantly reduced by increasing acid concentration. Increasing the concentration of organic additives increased the probability of abnormal growths (Figure 6(b)).

Due to this reason, we increased the acid concentration from the newly developed bath (while maintaining metal concentration constant and organic concentrations moderately low) with an expanse of LCD. As shown in Figure 7, we observed a significant change in morphology and growth shape from 7μm/min, which is much lower than that with a low acid bath. The growth shape changed significantly at high deposition rates due to an increased influence of mass transfer. This shows that bath LCD was the major limiting factor for this process, varying the morphology and growth shape at high %LCD. Other factors such as thickness and composition uniformity (WIW and WID) were acceptable up to the maximum deposition rate (6μm/min), which was determined by the morphology and growth shape.

Maximum achievable rate : 6μm/min
Primary limiting factors : abnormal growths and bath LCD

II. Cu Stud Deposition

Full details on the development of high-rate Cu stud deposition are summarized in Reference [16,21]. By increasing metal concentration and decreasing acid concentration, as in the eutectic SnPb bath, the deposition rates of 4-5μm/min were achieved (without the onset of abnormal growths) with an organic additive-free bath. However, surfaces were rough without organic additives. Various organic mixtures were tested to achieve smooth, flat, low-stressed deposits at high deposition rates [16,21]. Several defects associated with organic mixtures and their concentrations were observed at high deposition rates, as shown in Figure 8. Pores and local dendrites seemed to result from the high surface tension of the bath and local mass-transfer limitation. Irregular surfaces and crater-type defects were thought to result from the uneven adsorption of certain organic additives on surfaces, and rough surfaces were due to a poor grain-refining effect. Some organic mixtures produced highly stressed deposits, resulting in delamination. Severely domed or sloped profiles were also observed along the convective flow direction. In through-mask deposition, many factors affect the current distribution and growth shape of deposits [17-20, 22-25], but some organic mixtures produced more domed or sloped profiles at the same process conditions. Accordingly, we found that the poor functionality of organic components at high deposition rates was the first rate-limiting factor in copper stud deposition.

We selected the Intervia 8540 additive package after comparing a variety of organic mixtures [16]. This package contains three components; grain refiner (accelerator), wetting agent (strong suppressor), and leveler (weak suppressor). As shown in Figure 9, we saw no significant change in morphology and growth shape up to 5μm/min. However, we observed current crowding from the deposition rate of 4μm/min at the wafer edge and die corners, and severe current crowding at 5μm/min, which caused rougher deposits at those locations and poor WID thickness uniformity. Figure 10 shows the

variation of WID thickness uniformity as a function of deposition rate, where we measured 5 dice per wafer. The maximum deposition rate was limited to 4μm/min by current crowding at the wafer edge and die corners.

Maximum achievable rate : 4μm/min
Primary limiting factors : poor functionality of organic additives at high deposition rates and current crowding at the wafer edge and die corners

III. Ni Stud Deposition

After optimizing process conditions, we plated up to 7μm/min, which showed no severe change in growth shape and morphology. Figure 11 compares the morphology and growth shape at two different deposition rates. Scotch-tape pulling tests showed no delamination up to this deposition rate. In terms of thickness uniformity, WIW uniformity target (<10%, 3σ) was easily met, but WID uniformity became drastically worsened with increasing deposition rate. Figure 12 shows the variation of WID thickness uniformity as a function of deposition rate. The WID uniformity target (±15%, %range), which was looser than that of other processes, was barely met at 2-3μm/min. As this bath is based on nickel sulfamate with only one organic component working as a surfactant and thus has low conductivity, it has relatively worse throwing power than other baths (especially at high deposition rates).

Maximum achievable rate : 3μm/min
Primary limiting factors : WID thickness uniformity

IV. Eutectic SnAg Solder Deposition

Full details on the development of eutectic SnAg solder process are summarized in References [10,14]. We used insoluble anodes for this work due to the displacement reaction between silver ions and tin anodes in the bath [14]. Figure 13 shows the morphology and growth shape at two different deposition rates. The gas generation from the anodes became more severe with increasing deposition rate, and from the deposition rate of 3μm/min, gas generation started to greatly affect the deposit quality. As shown in Figure 13, very nonuniform deposits were achieved at 3μm/min; very thin deposits around the wafer center and very thick deposits at wafer edge. This phenomenon seems to result from bubble generation and trapping mostly around the wafer center, which causes nonuniform current distribution within a wafer. With another fountain-type reactor developed to accommodate soluble tin anodes without any significant displacement reaction, this problem was not observed and thus we can achieve much higher deposition rate (>3μm/min).

Maximum achievable rate : 2μm/min
Primary limiting factors : gas generation from insoluble anodes

Conclusions

We examined the important factors limiting the maximum deposition rate of various high-rate bump processes. The maximum rate of eutectic SnPb solder deposition was significantly reduced by the probability of abnormal growths. This problem was closely related to bath composition, which limited bath makeup and thus reduced the LCD and resultant maximum rate. The deposit qualities of Cu studs at high deposition rates were greatly affected by organic components and their concentrations. Many of the organic additives showed poor functionality at high deposition rates. With an optimized bath, the current crowding at high current density areas was the major limiting factor, causing poor WID thickness uniformity and rough deposits at high current density areas. Due to poor throwing power of Ni bath, WID thickness uniformity was barely acceptable even at low %LCD (2-3μm/min). Inert anodes were used for eutectic SnAg solder deposition to avoid a displacement reaction. Gas generation from the anodes significantly limited the operating range of current density. However, in all cases, we achieved acceptable rates with a tested pattern, ranging from 2 to 6μm/min depending upon process type.

References

[1] T. W. Goodman and E. J. Vardaman, "*FCIP and expanding markets for flip chip*", p. 2, TechSearch International, Inc., Austin, TX (1997).

[2] G. Solomon, TAP Technology, March, p. 29 (2001).

[3] M. Töpper and H. Reichl, Future Fab International, Issue 11, Test, Assembly and Packaging, Section 9 (2001).

[4] B. Ebersberger, R. Bauer, and L. Alexa, Future Fab International, Issue 17, Final Manufacturing, Section 9, p. 154 (2004).

[5] D-T. Chin, N. R. K. Vilambi, M. Sunkara, and D. Balamurugan, "*Selective pulse plating*", AESF Project #68 (1989).

[6] K. G. Sheppard and Q. Lin, "*Pulsed-electrodeposition of lead-tin solder alloys from a sulfonate bath*", AESF Project #88 (1995).

[7] M. Datta *et al.*, J. Electrochem. Soc., 142 (11), p. 3,779 (1995).

[8] K. Lin and Y. Liu, J. Electrochem. Soc., 150 (8), p. C529 (2003).

[9] B. Kim and T. Ritzdorf, J. Electrochem. Soc., 150 (2), p. C53 (2003).

[10] B. Kim and T. Ritzdorf, J. Electrochem. Soc., 150 (9), p. C577 (2003).

[11] B. Kim and T. Ritzdorf, J. Electrochem. Soc., 151 (5), p. C342 (2004).

[12] B. Kim and T. Ritzdorf, Chip Scale Review, March, p. 53 (2004).

[13] B. Kim and T. Ritzdorf, Proceedings of the 8th International Advanced Packaging Materials Symposium, p. 61, Stone Mountain, GA (2002).

[14] B. Kim, T. Ritzdorf, D. Schmauch, and P. Siblerud, "*Through-mask electrodeposition of leadfree solders for wafer-level packaging*", Proceedings of International Wafer Level Packaging Congress, San Jose, CA (2004).

[15] D. Landolt, Electrochim. Acta, 39, p. 1,075 (1994).

[16] B. Kim, T. Ritzdorf, S. Christian, and R. Forman, Solid State Technology, October, p. 57 (2004).

[17] B. Kim, T. Ritzdorf, C. Sharbono, and G. Saveskie, "*Effects of deposition conditions on the feature-scale growths of through-mask deposited metals*", The 206th Electrochemical Society (ECS) Meeting, Abstract 1,091, Honolulu, HI (2004).

[18] K. Kondo and K. Fukui, J. Electrochem. Soc., 145 (9), p. 3,007 (1998).

[19] M. Georgiadou, R. Mohr, and R. C. Alkire, J. Electrochem. Soc., 147 (8), p. 3,021 (2000).

[20] K. Hayashi, K. Fukui, Z. Tanaka, and K. Kondo, J. Electrochem. Soc., 148 (3), p. C145 (2001).

[21] B. Kim, D. Erickson, C. Sharbono, and T. Ritzdorf, "*Electro-chemically deposited copper for packaging applications*", IMAPS-ATW (Advanced Technology Workshop), Final Program and Abstract Book, Paper 14 (2003).

[22] K. Kondo, K. Fukui, K. Uno, and K. Shinohara, J. Electrochem. Soc., 143, p. 1,880 (1996).

[23] K. Kondo, K. Fukui, M. Yokoyama, and K. Shinohara, J. Electrochem. Soc., 144, p. 466 (1997).

[24] V. R. Subramanian and R. E. White, J. Electrochem. Soc., 149, p. C498 (2002).

[25] J. K. Luo, D. P. Chu, A. J. Flewitt, S. M. Spearing, N. A. Fleck, and W. I. Milne, J. Electrochem. Soc., 152 (1), p. C36 (2005).

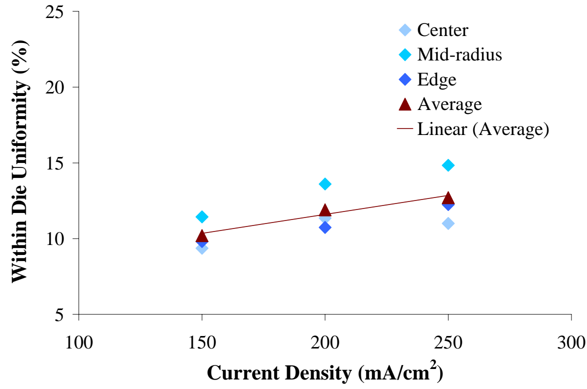

Figure 1. WID thickness uniformity of Cu studs as a function of current density.

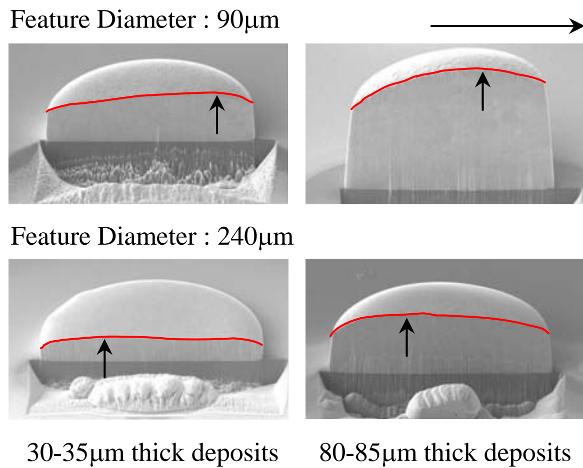

Figure 2. Effect of feature diameter and deposit thickness on the growth shape of Cu studs at high %LCD (60-70%), where the horizontal arrow indicates the average flow direction and the vertical arrow indicates the location of peak thickness within the feature; 100µm thick resist and 4µm/min.

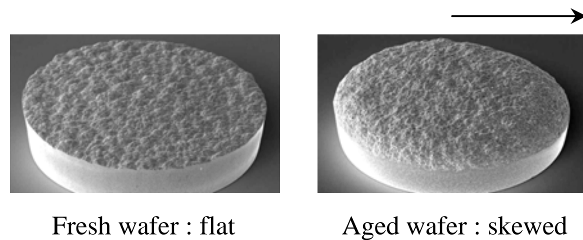

Figure 3. Effect of wafer aging on the feature-scale growths of eutectic SnPb bumps, where the arrow indicates the average flow direction; 4µm/min.

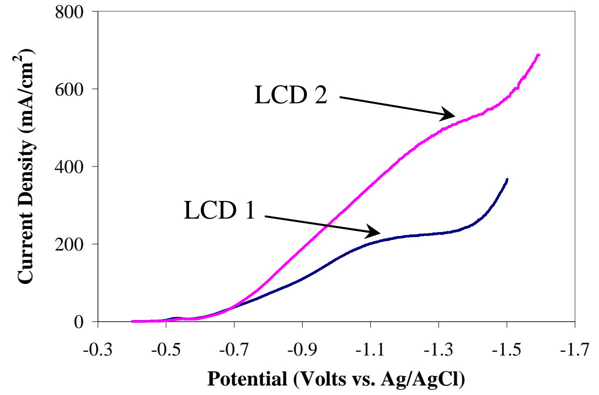

Figure 4. Comparison of LCD with two types of eutectic SnPb baths with different makeup.

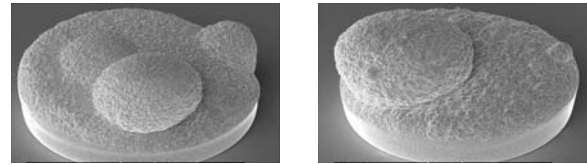

Figure 5. Abnormal growths of eutectic SnPb solder bumps; 4µm/min.

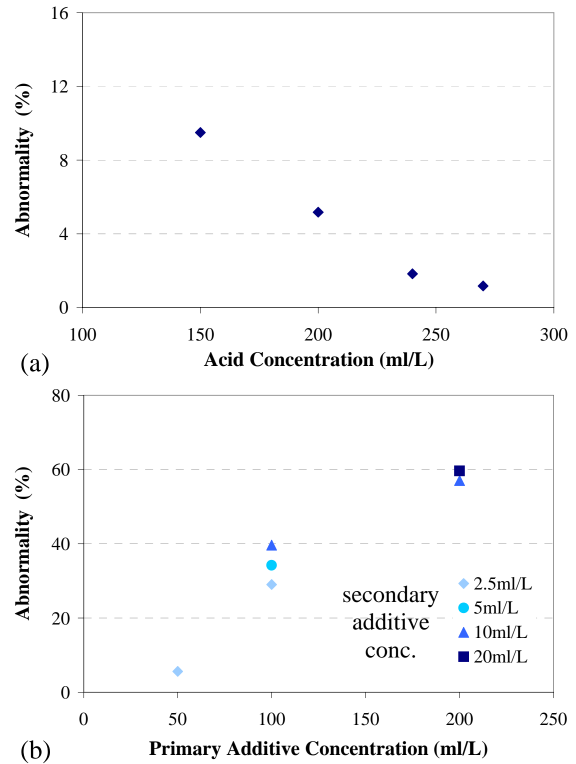

Figure 6. Effect of bath composition on the probability of abnormal growths: (a) effect of acid concentration; 4µm/min and low open area wafers and (b) effect of organic concentrations; 4µm/min, pattern-A, and low acid bath.

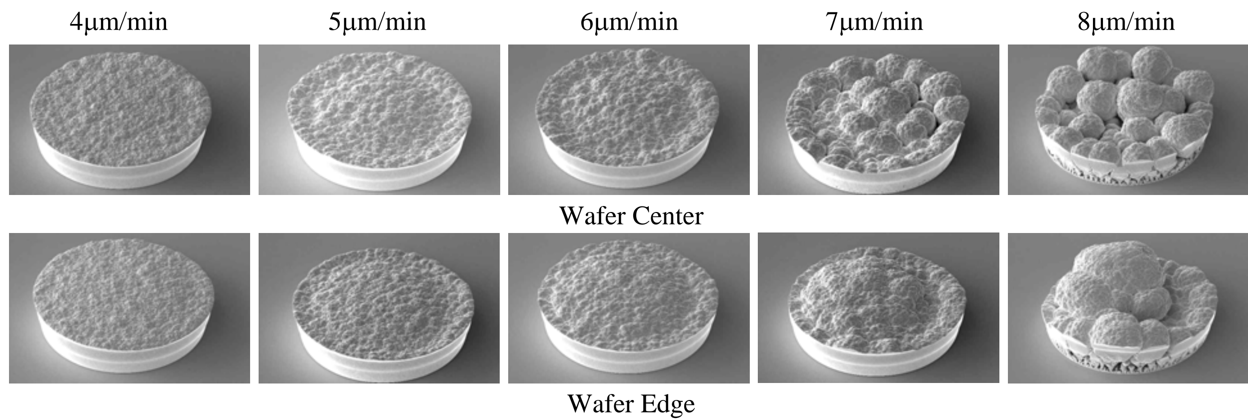

Figure 7. Effects of deposition rate on the morphology and growth shape of eutectic SnPb bumps.

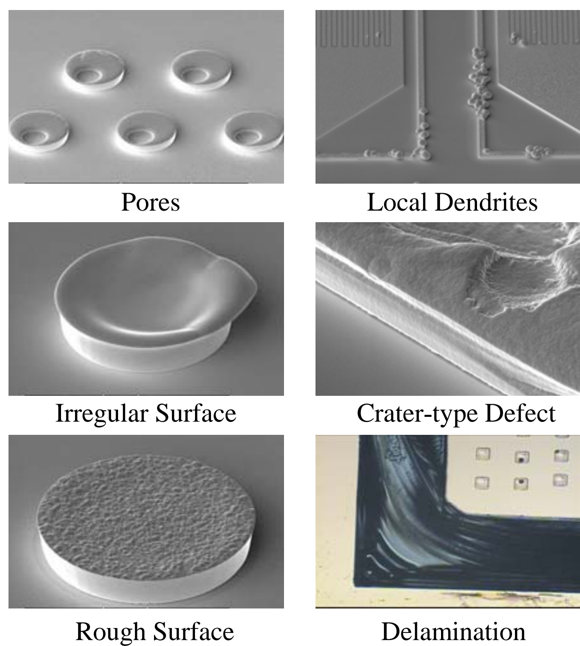

Figure 8. Typical defects in Cu deposition related with organic components and their concentrations; 3-4μm/min.

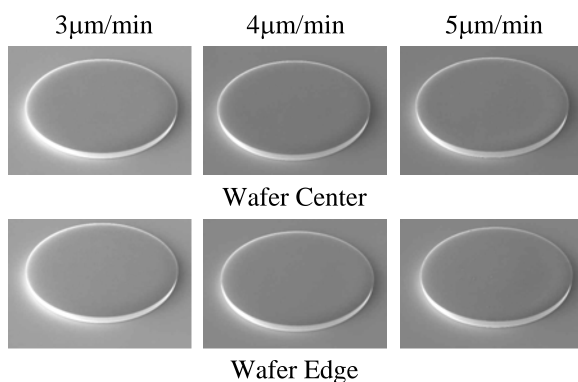

Figure 9. Surface morphology and growth shape of Cu studs at high deposition rates.

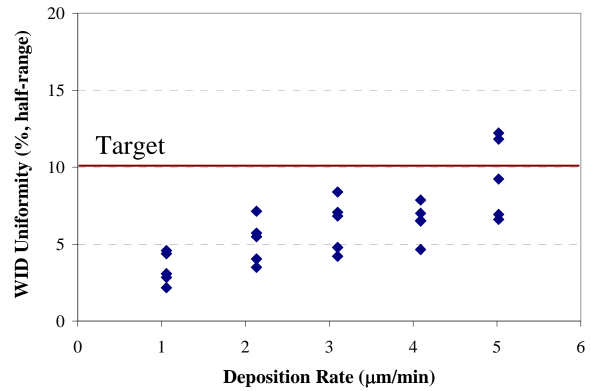

Figure 10. WID thickness uniformity of Cu studs as a function of deposition rate.

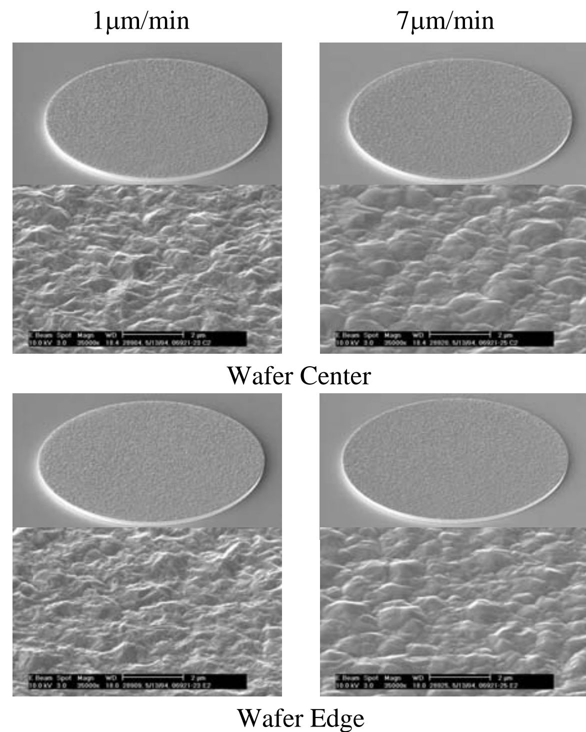

Figure 11. Surface morphology and growth shape of Ni studs as a function of deposition rate.

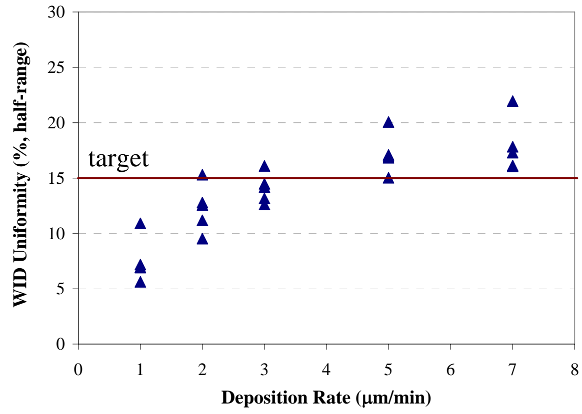

Figure 12. WID thickness uniformity of Ni studs as a function of deposition rate.

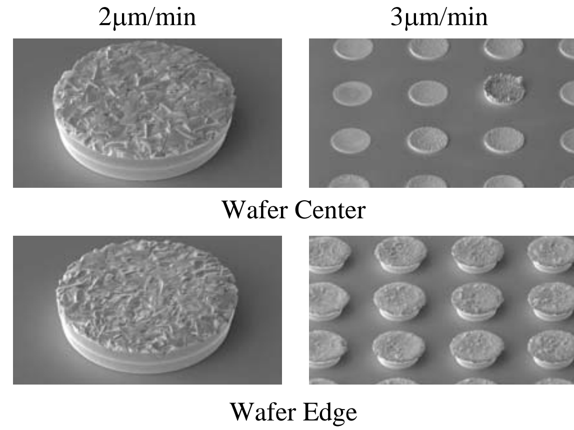

Figure 13. Surface morphology and growth shape of eutectic SnAg bumps as a function of deposition rate.